

Differential Oscillator

YSO230LR

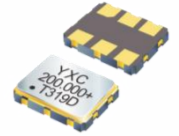


Applications

- Optical modules
- Accelerator Card

Features

- Frequency Range: 13.5MHz ~ 200MHz
- Package Size: 2.5*2.0, 3.2*2.5, 5.0*3.2 7.0*5.0mm
- Output: LVPECL, HCSL or LVDS



Specifications (规格参数)

Item/Type	LVPECL		LVDS		HCSL		Remarks
	7050/5032	3225/2520	7050/5032	3225/2520	7050/5032	3225/2520	
Output Frequency Range 额定频率范围	13.5 ~ 200 MHz	13.5 ~ 156.25 MHz	13.5 ~ 200 MHz	13.5 ~ 156.25 MHz	13.5 ~ 200 MHz	13.5 ~ 156.25 MHz	
Supply Voltage 电源电压	2.5V ~ 3.3V		1.8V, 2.5V ~ 3.3V		2.5V ~ 3.3V		
Operating Temperature Range 工作温度	-40~+85°C, or specify						
Storage Temperature Range 储存温度	-55~+125°C						
Total Stability 频率偏差	±25ppm, ±50ppm, or specify						Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature
Current Consumption 消耗电流	80mA Max	50mA Max	60mA Max	40mA Max	50mA Max		OE=VDD, LVPECL=(50)Ω, HCSL=(50)Ω or LVDS=(100)Ω
Disable Current 禁用电流	10uA Max						OE=GND
Output Voltage (LVPECL) 输出电压 (LVPECL)	VOH=VDD-1.03 Min		--		--		DC characteristics
	VOL=VDD-1.6 Max		--		--		
Output Voltage (LVDS) 输出电压 (LVDS)	--		VOH=1.6 Max		--		DC characteristics
	--		VOL=0.9 Min		--		
Output Voltage (HCSL) 输出电压 (HCSL)	--		--		VOH= 0.9V Max		DC characteristics
	--		--		VOL= -0.15V Min		
Output Load Condition 输出负载	L_PECL=50Ω		--		--		Terminated to VDD-2.0V
	--		L_LVDS=100Ω		--		Connected between OUT to OUT
	--		--		L_HCSL=50Ω		--
Input Voltage 输入电压	VIH=70% VDD Min, VIL=30%VDD Max						OE terminal
Duty Cycle 占空比	45~55%						
Rise Time/Fall Time 上升沿/下降沿	0.8nS Max				0.7nS Max		LVPECL: Between 20% and 80% of (VOH-VOL), LVDS: Between 20% and 80% Differential Output peak to peak voltage

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Item/Type	LVPECL		LVDS		HCSL		Remarks
	7050/5032	3225/2520	7050/5032	3225/2520	7050/5032	3225/2520	
Start-up time 启动时间	10mS						Time at minimum supply voltage to be 0 s
Aging 老化率	±3ppm						25°C First year, VDD=2.5V, 3.3V
RMS Jitter [12 kHz ~ 20 MHz] 相位抖动	100MHZ	125MHZ	148.5MHZ	156.25MHZ	180MHZ	200MHZ	
	0.3ps Typ.	0.1ps Typ.					

Pin Dimension (脚位尺寸)

Pin	#1	#2	#3	#4	#5	#6
FUNCTION	OE	NC	GND	OUT+	OUT-	VDD

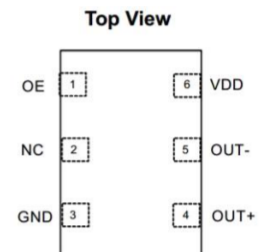


Figure 1. Pin Assignments

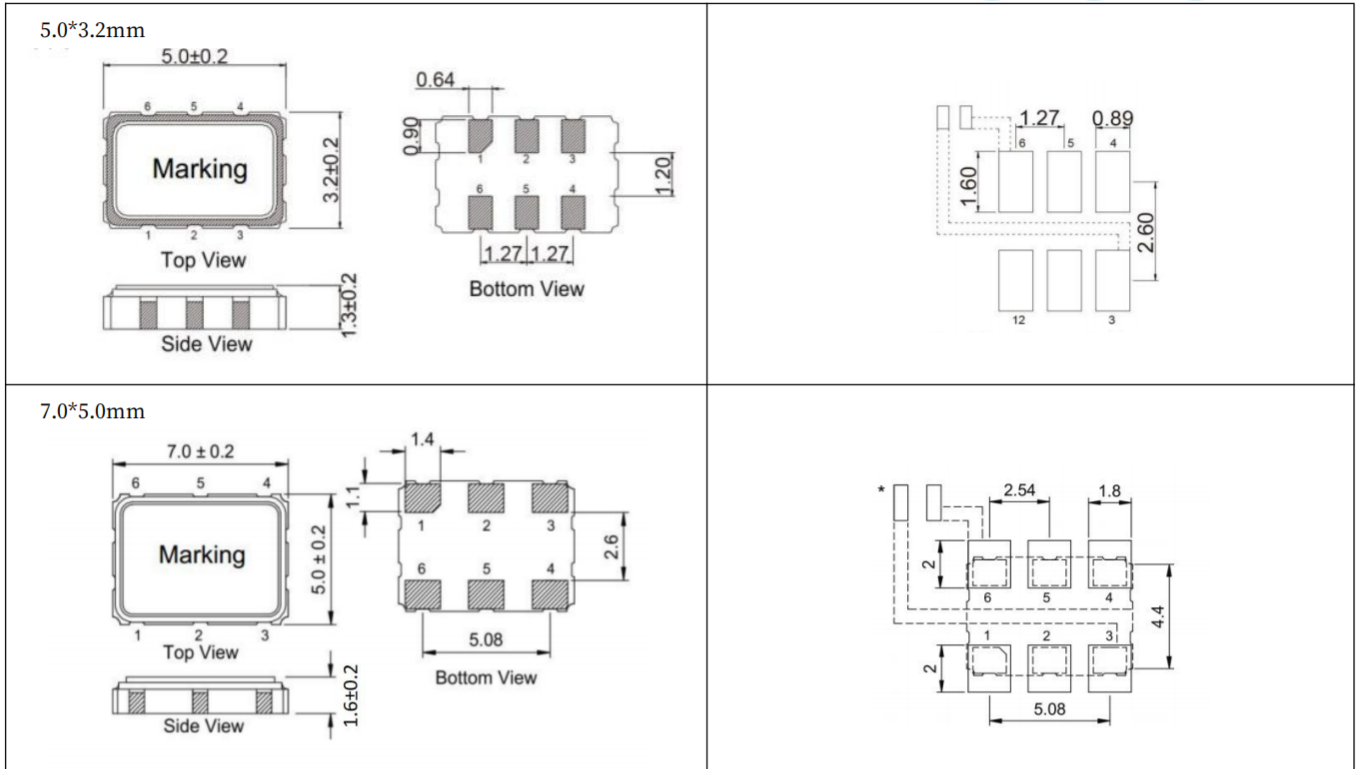
Notes: To maintain stable operation provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between VDD-GND).

Dimensions and Recommended Land Pattern (外观尺寸及推荐焊盘)

Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>2.5*2.0mm</p>	
<p>3.2*2.5mm</p>	

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Notes:

1.A capacitor of value 0.01uf-0.1uf or higher between VDD and GND is required.

Test Circuit (测试电路)

