

Programmable Temperature Compensated YSO511PJ TCXO



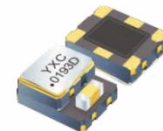
Applications

- Networking
- Industrial

Features

- Fast Delivery
- Performance of 0.8pS RMS

- Low Jitter Design with New Developed IC
- Package Size: 3.2*2.5mm, 7.0*5.0mm



Specifications (规格参数)

Item / Type	CMOS	
Frequency Range 额定频率范围	10MHz ~ 250MHz	
Supply Voltage VDD 电源电压	2.5V, 3.3V	
Operating Temperature Range 工作温度	-40~+85°C, or specify	
Storage Temperature Range 储存温度	-55~+150°C	
Output Type 输出方式	CMOS	
Rise Time / Fall Time (Tr / Tf : 10% ↔ 90% waveform) 上升沿/下降沿	1.5nsec (typ.) 3.0nsec (max.)	
Duty Cycle 占空比	45~55%	
Voltage VOH (Min.) / VOL (Max.) 输出电压	VOH = 90%VDD / VOL = 10%VDD	
Start-up Time 启动时间	5.0msec (max.)	
Output Load 输出负载	15pF	
RMS Jitter [12 kHz ~ 20 MHz] 相位抖动	0.8psec (typ.)	
Current Consumption (Max.) 消耗电流	Vdd=2.5V	Vdd=3.3V
	50MHz : 34mA	50MHz : 36mA
	125MHz : 38mA	125MHz : 40mA
200MHz : 40mA	200MHz : 44mA	
Current with Output Disabled 禁用电流	18mA (typ.)	
Initial Calibration Tolerance 初始校准公差	±2.0 ppm (max.) at +25°C ±2°C (at the shipment)	
Voltage VOH (Min.) / VOL (Max.) 输入电压	70% of VDD (min.) to enable output (Open connection prohibit.)	
	30% of VDD (max.) to disable output	

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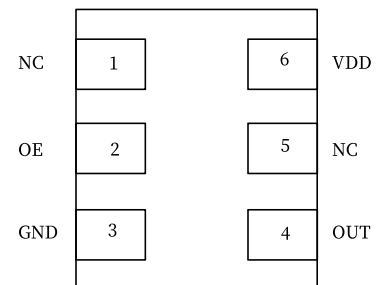


Frequency Stability 频率偏差	Temperature (ref to +25°C)				± 2.5 ppm over -30°C to +85°C (default)			
					± 1.0 ppm over -40°C to +85°C (available)			
	Aging at Ta = +25°C				± 2.0 ppm max, first year at 25°C			
	Voltage Change				± 0.2 ppm max, for a ±5% input voltage change			
Frequency Stability 频率偏差	Load Change				± 0.2 ppm max, for a ±10% load condition change			
	Reflow				± 1.0 ppm max, 1 reflow and measured 24 hours afterwards			
Phase Noise[dBc / Hz (Typical)] 相位噪声	Offset	10Hz	100Hz	1KHz	10KHz	100KHz	1MHz	10MHz
	125MHz	-51	-93	-111	-123	-125	-135	-155
	212.5MHz	-42	-87	-105	-115	-118	-130	-151
	312.5MHz	-49	-88	-107	-111	-114	-124	-147

Pin Dimension (脚位尺寸)

Pin	#1	#2	#3
FUNCTION	No Connection	Out Enable	Ground
Pin	#4	#5	#6
FUNCTION	Output	No Connection	Supply Voltage

Pin Assignments

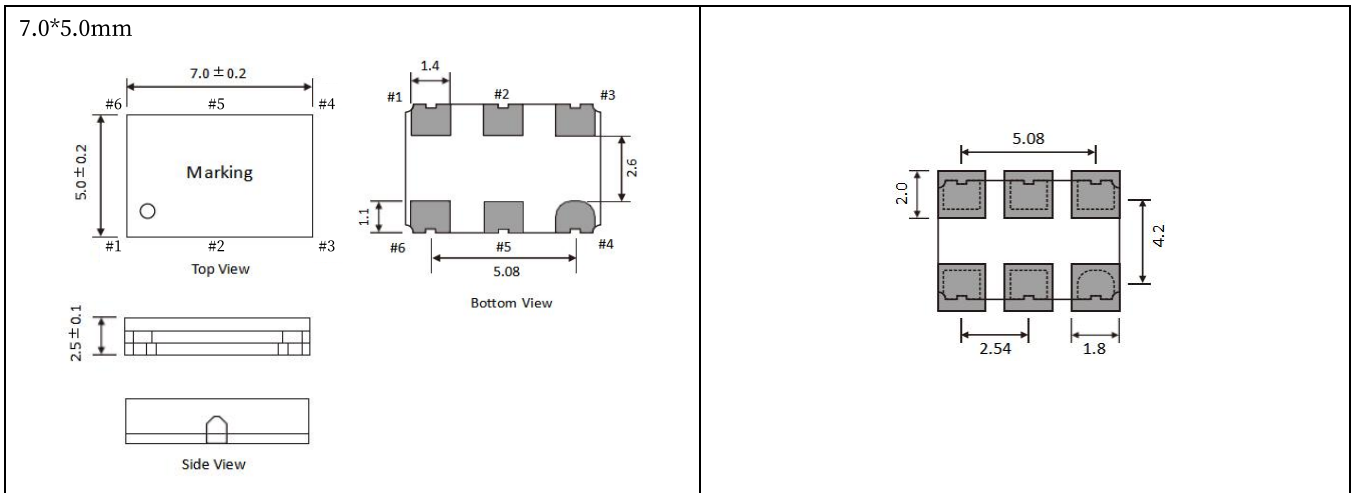


Top View

Dimensions and Recommended Land Pattern (外观尺寸及推荐焊盘)

Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>3.2*2.5mm</p> <p>The left diagram shows the physical dimensions of the component in three views: Top View, Bottom View, and Side View. The top view shows a rectangular package with a central marking area. Dimensions include a total width of 3.2 ± 0.1 mm, a total height of 2.5 ± 0.1 mm, and a marking area width of 2.0 ± 0.2 mm. Pin positions are labeled #1 through #6. The bottom view shows the component's profile with a height of 1.6 ± 0.1 mm. The right diagram shows the recommended land pattern for the component, with dimensions for the pads: a central pad of 1.6 mm by 2.0 mm, and four side pads each 0.75 mm wide and 1.1 mm high. The pads are spaced 1.28 mm apart.</p>	

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Test Circuit (测试电路)

